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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/734,927 | 12/12/2003 | Imtiaz Khan | 49188/RAG/L400 | 2227 |

23363 7590 05/12/2005

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| EXAMINER | |
|---|---|
| NGUYEN, SANG H | |
| **ART UNIT** | **PAPER NUMBER** |
| 2877 | |

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/734,927 | KHAN ET AL. | |
| | Examiner | Art Unit | |
| | Sang Nguyen | 2877 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

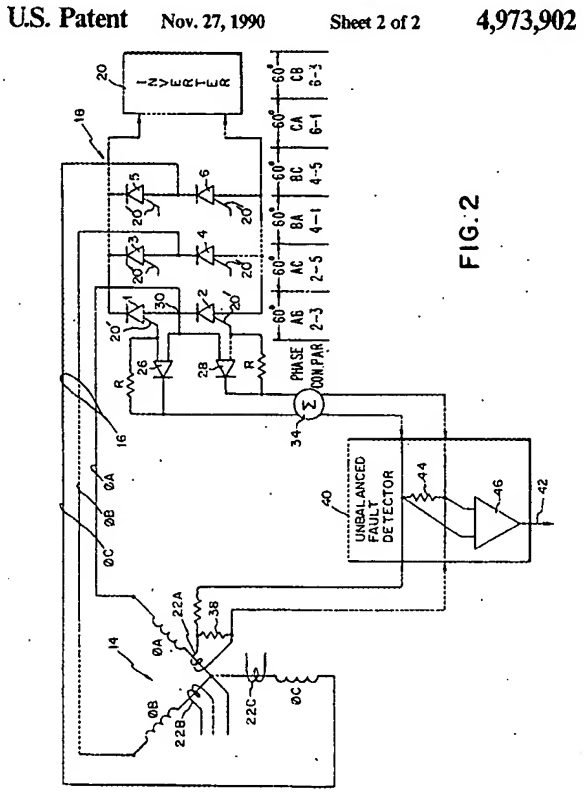
> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claim 1 are rejected under 35 U.S.C. 102(b) as being anticipated by Dhyanchand et al (U.S. Patent No. 4,973,902).**

**Regarding claim 1**; Dhyanchand et al discloses all of features claimed invention as to indicate an arc fault detector for detecting arc faults in three phase load aircraft power system (14 of figure 2 and col. 1 lines 7-32), comprising:

- a generator means (14 of figure 2) for generating a signal indicative of each (Φa, Φb, Φc of figure 2) of the three phase (14 of figure 2);
- three full wave rectifier means (18 of figure 2) for generating the signal indicative of each (Φa, Φb, Φc of figure 2) of the three phase (14 of figure 2) , wherein each having an output connected to a threshold detector considered to be a current sensing or sensor (20' of figure 2);
- three input comparator means considered to each of three operational amplifiers (26, 28 of figure 2) connected to a summing junction (34 of figure 2) connected to an output of the threshold detector (20 of figure 2); and
- a fault verification circuit means considered to be an unbalance fault detector (40 of figure 2) connected to an output of the three input comparator (26, 28, 34 of figure

2) and for generating a signal (42 of figure 2 and col.2 lines 62 to col.3 line 3) in response to three rectified signals from the three input comparator means (26, 28 of figure 2). See claims 1-6 and figures 1-2.




**Regarding claim 4**; Dhyanchand et al teaches of the three input comparator (have three operational amplifier [26, 28 of figure 2] connected three full wave rectifiers [18 of figure 2]) for generating a signal indicative of the outputs of any two of the

threshold detectors (20' of figure 2) differing by more than a predetermined amount (col.2 line 57 to col.3 line 3).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claims 2, 6-11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhyanchand et al (U.S. Patent No. 4,973,902) in view of Chen et al (U.S. Patent No. 4,347,541).**

**Regarding claim 2**; Dhyanchand et al discloses all of features claimed invention except for a first input connected to an output of one of full wave rectifiers, a second input connected to a signal indicative of a predetermined threshold and an output. However, Chen et al teaches that it is known in the art to provide a first comparator (66 of figure 3) having a first input connected to an output of one of full wave rectifiers (16 of figure 3), a second input connected to a signal indicative of a predetermined threshold (67, 68 of figure 3) and an output (figure 3) to connected to OR circuit (26 of figure 3 and col.7 lines 22-45). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify an arc fault detector for detecting arc faults in three phase load aircraft power system of Dhyanchand et al with a first input connected to an output of one of full wave rectifiers, a second input connected to a signal indicative of a predetermined threshold and an output as taught by Chen et al

for the purpose of improving the circuit breaker having current sensing, signal processing circuits and a tripping circuit for better.

**Regarding claims 6, 8-11, and 14;** Dhyanchand et al discloses all of features claimed invention as to indicate an arc fault detector for detecting arc faults in three phase load aircraft power system (14 of figure 2 and col. 1 lines 7-32), comprising:

- a generator means (14 of figure 2) for generating a signal indicative of each (Φa, Φb, Φc of figure 2) of the three phase (14 of figure 2);
- three full wave rectifier means (18 of figure 2) for generating the signal indicative of each (Φa, Φb, Φc of figure 2) of the three phase (14 of figure 2) , wherein each having an output connected to a threshold detector considered to be a current sensing or sensor (20' of figure 2);
- three input comparator means considered to each of three operational amplifiers (26, 28 of figure 2) connected to a summing junction (34 of figure 2) connected to an output of the threshold detector (20 of figure 2); and
- a fault verification circuit means considered to be an unbalance fault detector (40 of figure 2) connected to an output of the three input comparator (26, 28, 34 of figure 2) and for generating a signal (42 of figure 2 and col.2 lines 62 to col.3 line 3) in response to three rectified signals from the three input comparator means (26, 28 of figure 2). See claims 1-6 and figures 1-2.

Dhyanchand et al discloses all of features claimed invention except for a detected signal indicative of at least two of the three rectified signals differing for a time period exceeding a predetermined duration by the fault verification circuit means,

wherein the detection of differences having continuously monitoring and sampling the signals indicative of the three phase. However, Chen et al teaches that it is known in the art to provide fault verification circuit means considered to be an output stage (13 of figure 1) for generating a detected signal indicative of at least two considered to be a long term delay signal, a short term delay signal, or an instantaneous trip signal of the three rectified signal differing for a time period exceeding a predetermined duration (col.8 lines 19-34), wherein the detection of differences having continuously monitoring and sampling the signals indicative of the three phase (col.7 lines 20-67). See figures 1-7.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify an arc fault detector for detecting arc faults in three phase load aircraft power system of Dhyanchand et al with a detected signal indicative of the three rectified signal differing for a time period exceeding a predetermined duration by the fault verification circuit means, wherein the detection of differences having continuously monitoring and sampling the signals indicative of the three phase as taught by Chen et al for the purpose of detecting a signal with less sensitive in a noisy environment and high reliability and precise time control for better coordination with downstream breakers.

**Regarding claim 7**; Dhyanchand et al discloses all of features claimed invention except for means for detecting one of three rectified signals exceeds a predetermined threshold. However, Chen et al teaches a threshold detection means (66 of figure 3 and col.7 lines 22-46) for detecting one of three rectified signals exceeds a predetermined

threshold. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify an arc fault detector for detecting arc faults in three phase load aircraft power system of Dhyanchand et al with means for detecting one of three rectified signals exceeds a predetermined threshold as taught by Chen et al for the purpose of adjusting threshold setting for determining the instantaneous trip is activated and less sensitive in a noisy environment in system.

**Claims 3, 5, and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhyanchand et al in view of Chen et al as applied to claims 1-2 above, and further in view of Demeyer et al (U.S. Patent No. 4,571,659).**

**Regarding claims 3 and 12-13**; Dhyanchand et al in view of Chen et al discloses all of features claimed invention except for an integrator in the threshold detector configured to integrate the output of the first comparator comparing the magnitude generated signals indicative of each of three phase to a predetermined threshold and generating a signal for each phase indicative of the magnitude of the signal relative to the threshold. However, Demeyer et al teaches that it is known in the art to provide an integrator (12 of figures 1-56 and col. 2 lines 10-20 and 55-68) in the threshold detector (figure s 6-7) configured to integrate the output of the first comparator (14 of figures 1-5) for comparing the magnitude generated signals indicative of each of three phase to a predetermined threshold and generating a signal for each phase indicative of the magnitude of the signal relative to the threshold (col.2 lines 1-30). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify an arc fault detector for detecting arc faults in three phase load

aircraft power system of Dhyanchand et al with an integrator in the threshold detector configured to integrate the output of the first comparator comparing the magnitude generated signals indicative of each of three phase to a predetermined threshold and generating a signal for each phase indicative of the magnitude of the signal relative to the threshold as taught by Demeyer et al for the purpose of modifying accurately of the integrator time constant takes place by varying the value of the negative feed back capacitor C.

**Regarding claim 5**; Dhyanchand et al discloses all of features claimed invention except for an integrator in the fault verification circuit connected to the output of three input comparator and a comparator connected to output the integrator and configured to generate a signal indicative of the detection of fault when the output of the integrator exceeds a predetermined threshold. However, Demeyer et al teaches that it is known in the art to provide an integrator(C2 of figure 7) of integrating amplifier (14 of figure 7) in the fault verification circuit (32 of figure 7) connected to the output of three input comparator (A1, A3 of figure 7) and a comparator (18 of figure 7) connected to output the integrator (14 of figure 7) and configured to generate a signal indicative of the detection of fault when the output of the integrator exceeds a predetermined threshold (col.5 line 65 to col.6 line 68). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify an arc fault detector for detecting arc faults in three phase load aircraft power system of Dhyanchand et al with an integrator in the threshold detector configured to integrate the output of the first comparator as taught by Demeyer et al for the purpose of modifying accurately of the

integrator time constant takes place by varying the value of the negative feed back capacitor C.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Schmalz et al (5933305) discloses arc fault detector comparing integrated interval to interval filtered load current; Udren (4862308) teaches power bus fault detection and protection system; Jahns et al (4777579) discloses integrated current sensor configuration for ac motor drives; Engelmann et al (4673888) discloses power control system; Cutler et al (4589050) discloses method and apparatus for the protection of a thyristor power conversion system; Schoenmeyr (4333119) discloses power monitor system; Knauner (3982158) discloses power distribution control system; or Hoss (3700967) discloses ground fault detection circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sang Nguyen whose telephone number is (571) 272-2425. The examiner can normally be reached on 9:30 am to 7:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory J. Toatley, Jr. can be reached on (571) 272-2800 ext. 77. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SN

Sang Nguyen/SN

May 7, 2005

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**Supervisory Patent Examiner**
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10/May/05